74AHC139-Q100; 74AHCT139-Q100

Dual 2-to-4 line decoder/demultiplexer

Rev. 3 — 7 September 2023

Product data sheet

1. General description

The 74AHC139-Q100; 74AHCT139-Q100 decodes two binary weighted address inputs (nA0, nA1) to four mutually exclusive outputs (n \overline{Y} 0 to n \overline{Y} 3). Each decoder features an enable input (n \overline{E}). When n \overline{E} is HIGH all outputs are forced HIGH. The enable input can be used as the data input for a 1-to-4 demultiplexer application. Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 to 5.5 V
- · Balanced propagation delays
- · High noise immunity
- · CMOS low power dissipation
- · All inputs have Schmitt-trigger actions
- Overvoltage tolerant inputs to 5.5 V
- Input levels:
 - For 74AHC139-Q100: CMOS level
 - For 74AHCT139-Q100: TTL level
- · Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

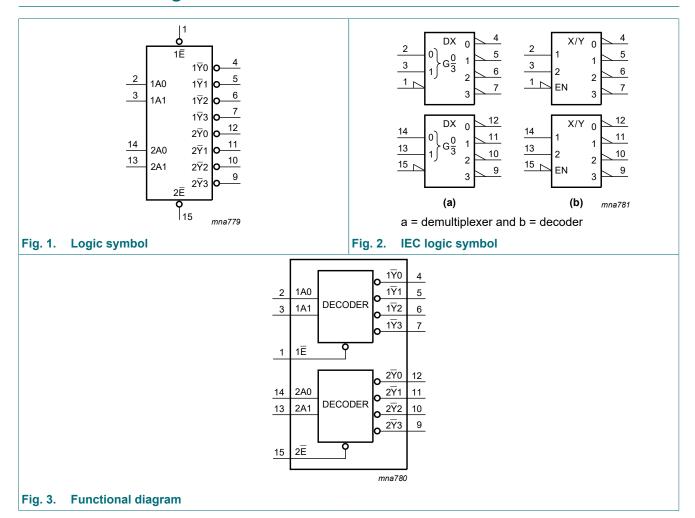
3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC139D-Q100 74AHCT139D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AHC139PW-Q100 74AHCT139PW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

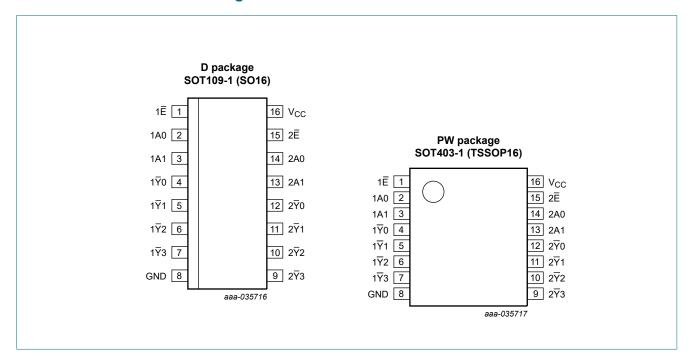


4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Table 2. Fill description		
Symbol	Pin	Description
1E, 2E 1, 15		enable input (active LOW)
1A0, 1A1	2, 3	address input
1₹0, 1₹1, 1₹2, 1₹3	4, 5, 6, 7	output
GND	8	ground (0 V)
2₹3, 2₹2, 2₹1, 2₹0	9, 10, 11, 12	output
2A1, 2A0	13, 14	address input
V _{CC}	16	supply voltage

6. Functional description

Table 3. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level; \ X = don't \ care.$

Control	Input		Output						
nΕ	nA0	nA1	n ₹0	n ₹1	n ₹2	n ₹3			
Н	X	Х	Н	Н	Н	Н			
L	L	L	L	Н	Н	Н			
	Н	L	Н	L	Н	Н			
	L	Н	Н	Н	L	Н			
	Н	Н	Н	Н	Н	L			

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
VI	input voltage		-0.5	+7.0	V
I _{IK}	input clamping current	$V_{I} < -0.5 V$ [1]	-20	-	mA
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$ [1]	-20	+20	mA
Io	output current	$V_{\rm O} = -0.5 \text{ V to } (V_{\rm CC} + 0.5 \text{ V})$	-25	+25	mA
I _{CC}	supply current		-	+75	mA
I_{GND}	ground current		-75	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$ [2]	-	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
74AHC1	39-Q100	'				
V_{CC}	supply voltage		2.0	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 3.0 V to 3.6 V	-	-	100	ns/V
		V _{CC} = 4.5 V to 5.5 V	-	-	20	ns/V
74AHCT	139-Q100	'				
V _{CC}	supply voltage		4.5	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 4.5 V to 5.5 V	-	-	20	ns/V

^[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C. For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C	;	-40 °C t	o +85 °C	-40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74AHC1	39-Q100								-	
V _{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL}	LOW-level	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OH}	HIGH-level	V _I = V _{IH} or V _{IL}								
	output voltage	I _O = -50 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -50 μA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = -50 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_{O} = -4.0 mA; V_{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I_{O} = -8.0 mA; V_{CC} = 4.5 V	3.94	-	-	3.80	-	3.70	-	V
V _{OL}	LOW-level	V _I = V _{IH} or V _{IL}								
	output voltage	I _O = 50 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu A; V_{CC} = 3.0 V$	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		$I_O = 8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
l _l	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	μΑ
C _I	input capacitance	V _I = V _{CC} or GND	-	3	10	-	10	-	10	pF
Co	output capacitance		-	4	-	-	-	-	-	pF

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74AHCT	139-Q100		'							'
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I _O = -50 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -8.0 mA	3.94	-	-	3.80	-	3.70	-	V
V _{OL} LOW-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$									
	output voltage	Ι _Ο = 50 μΑ	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μΑ
Icc	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	4.0	-	40	-	80	μΑ
ΔI _{CC}	additional per input pin; $ V_I = V_{CC} - 2.1 \text{ V}; $ other pins at V_{CC} or GND; $ I_O = 0 \text{ A}; $ $ V_{CC} = 4.5 \text{ V} \text{ to } 5.5 \text{ V} $		-	-	1.35	-	1.5	-	1.5	mA
Cı	input capacitance	V _I = V _{CC} or GND	-	3	10	-	10	-	10	pF
Co	output capacitance		-	4	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

Symbol	Parameter	Conditions		25 °C		-40 °C to	o +85 °C	-40 °C to	+125 °C	Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
74AHC1	39-Q100				'				-	
t _{pd}		nAn to n∀n; see <u>Fig. 4</u> [2]								
	delay	V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF	-	5.5	11.0	1.0	13.0	1.0	14.0	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF	-	7.9	14.5	1.0	16.5	1.0	18.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	-	3.9	7.2	1.0	8.5	1.0	9.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	5.6	9.2	1.0	10.5	1.0	11.5	ns
		nĒ to nŸn; see <u>Fig. 5</u> [2]								
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	-	4.8	9.2	1.0	11.0	1.0	11.5	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF	-	6.9	12.7	1.0	14.5	1.0	16.0	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	3.4	6.3	1.0	7.5	1.0	8.0	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	4.9	8.3	1.0	9.5	1.0	10.5	ns
C _{PD}	power dissipation capacitance	$f_i = 1 \text{ MHz}; V_i = \text{GND to } V_{CC}$ [3]	-	26	-	-	-	-	-	pF
74AHCT	139-Q100; V	_{CC} = 4.5 V to 5.5 V								
t _{pd}	propagation	nAn to $n\overline{Y}n$; see Fig. 4 [2]								
	delay	C _L = 15 pF	-	4.7	7.2	1.0	8.5	1.0	9.0	ns
		C _L = 50 pF	-	6.5	9.2	1.0	10.5	1.0	11.5	ns
		nE to nYn; see Fig. 5 [2]								
		C _L = 15 pF	-	3.6	6.3	1.0	7.5	1.0	8.0	ns
		C _L = 50 pF	-	5.2	8.3	1.0	9.5	1.0	10.5	ns
C _{PD}	power dissipation capacitance	$f_i = 1 \text{ MHz}; V_i = \text{GND to } V_{CC}$ [3]	-	23	-	-	-	-	-	pF

Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$$
 where:

 f_i = input frequency in MHz;

fo = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching; $\Sigma (C_L \times V_{CC}^{\ 2} \times f_o) = sum \ of \ the \ outputs.$

t_{pd} is the same as t_{PLH} and t_{PHL}. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W). P_D = C_{PD} × V_{CC} 2 × f_i × N + Σ (C_L × V_{CC} 2 × f_o) where:

10.1. Waveforms and test circuit

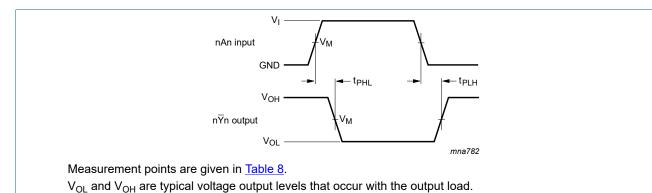


Fig. 4. Address input to output propagation delays

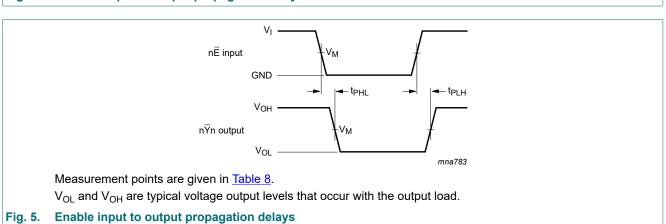
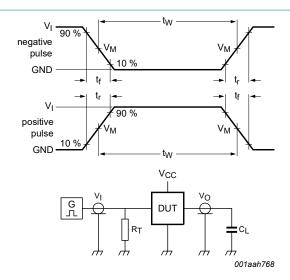


Table 8. Measurement points

Туре	Input	Output
	V _M	V _M
74AHC139-Q100	0.5 × V _{CC}	0.5 × V _{CC}
74AHCT139-Q100	1.5 V	0.5 × V _{CC}



Test data is given in Table 9.

Definitions test circuit:

 R_{T} = termination resistance should be equal to output impedance Z_{o} of the pulse generator;

 C_L = load capacitance including jig and probe capacitance.

Fig. 6. Test circuit for measuring switching times

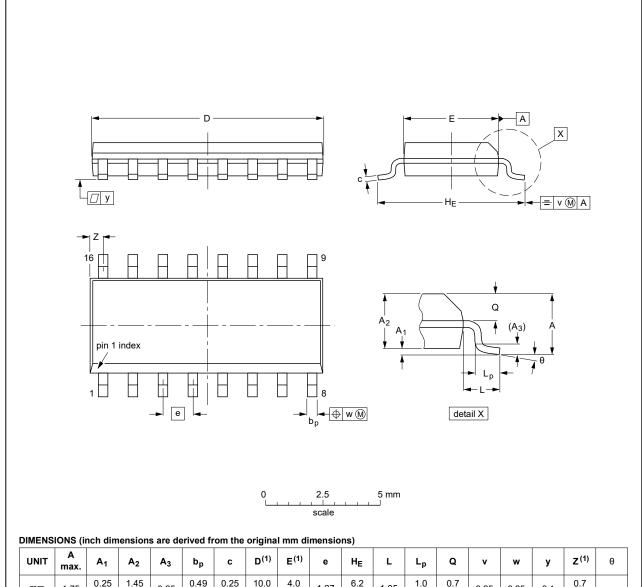
Table 9. Test data

Туре	Input		Load	Test
	VI	t _r , t _f	C _L	
74AHC139-Q100	V _{CC}	≤ 3.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}
74AHCT139-Q100	3.0 V	≤ 3.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075		0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	0°

Note

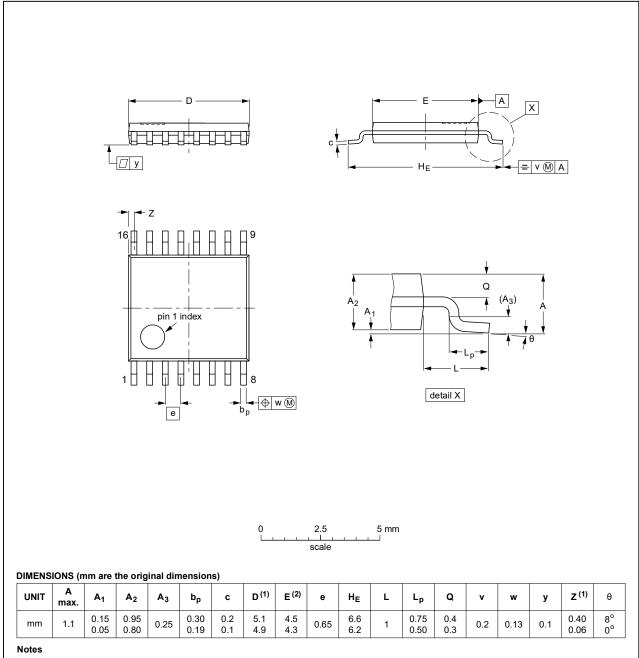
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT109-1	076E07	MS-012			99-12-27 03-02-19

Fig. 7. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE	REFERENCES			EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT403-1		MO-153				99-12-27 03-02-18

Fig. 8. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT139_Q100 v.2	20230907	Product data sheet	-	74AHC_AHCT139_Q100 v.1
Modifications	guidelines o Legal texts I Section 1 up Section 2: u	nave been adapted to the rodated.	new company nan	ne where appropriate. g to the latest JEDEC standard.
74AHC_AHCT139_Q100 v.1	20130605	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] Production data sheet		This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
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